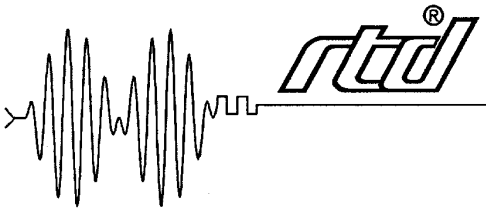
GPS6160HR
12 Channel GPS Receiver Module

User's Manual

Hardware revision 1.1



Real Time Devices, Inc.

"Accessing the Analog World"®

GPS6160HR
12 Channel GPS Receiver Module
User's Manual

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WARNING

LIFE SUPPORT APPLICATIONS

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Notice: We have attempted to verify all information in this manual as of the publication date. Information in this manual may change without prior notice from RTD Finland Oy.

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Chapter 1 - INTRODUCTION

This user's manual describes the operation of the RTD GPS6160HR integrated low power fast fix GPS module designed for mobile, marine, and automotive applications.

Features

Some of the key features of the GPS6160HR include:

- 12-channel low power Fastrax iTrax02 GPS receiver
- NMEA and binary protocols
- +3,3V and +5V active GPS antenna support
- 16C550 UART interface to host computer
- Supports COM1,COM2,COM3,COM4 or COMx
- Available IRQ's 2,5,6,7,10,11,12,14,15
- Status LED's indicating GPS activity and status
- 16 TTL I/O's 8 outputs 8 inputs
- +5V only operation, 1.3W typical
- Wide operating temperature range –40 to + 85C guaranteed
- Fully PC/104 compliant, IDAN versions available

The following paragraphs briefly describe the major features of the GPS6160HR. A more detailed discussion is included in Chapter 4 (Hardware description) The boards installation is described in Chapter 2 (Board Installation).

GPS receiver

Integrated on your GPS6160HR is a fast fix 12-channel low power iTrax02 GPS receiver from Fastrax. This new receiver will work reliably in a variety of installations. The receiver will work with either 3,3V or 5,0V active or with passive antennas. The power consumption of the GPS receiver is 125mW fully operational. A fast 1 to 4Hz updating rate is achieved using the binary iTalk protocol. Two output formats are available: the NMEA-0183 ASCII protocol or the iTalk proprietary binary protocol. Swiching between these protocols is controlled with one bit in the internal board registers.

16C550 compatible UART

Communication to the GPS6160HR board is performed through a standard 16C550 compatible UART. This onboard serial port leaves other system serial ports free for the user. All operating systems will recognize and support this standard UART, and therefore no special communication drivers are needed to receive data from your GPS6160HR board. The

address and interrupt of your serial channels can be individually set with the onboard jumper fields.

I/O interfaces

The GPS6160HR can be controlled and monitored from the software through two dedicated I/O registers. A special I/O connector is available for the user to connect to the general-purpose TTL level digital I/O.

Mechanical description

The GPS6160HR is designed on a PC/104 form factor. An easy mechanical interface to both PC/104 and RTD IDAN systems can be achieved. Stack your GPS6160HR directly on a PC/104 compatible CPU module using the onboard mounting holes and standoffs.

Connector description

The GPS antenna interface uses an OSX type miniature coaxial connector. Connect your antenna directly to the GPS6160HR antenna connectors, or use a short cable inside your enclosure to connect to a feed through connector to allow connection of the antennas to the wall of your enclosure. All I/O connections are made using header type terminals.

What comes with your board

Your GPS6160HR package contains the following items:

- GPS6160HR board
- User's manual

Note: Device drivers and example software available on our website

If any item is missing or damaged, please send an EMAIL to Real Time Devices Finland sales service department at Internet address: <sales@rtdfinland.fi>.

Note that RTD Finland also can offer a GPS6160HR starter kit that will include an active antenna with ready cables for direct evaluation and testing of this module. The part number for this starter kit is ***SK-GPS6160HR***.

Using this manual

This manual is intended to help you install your new GPS6160HR module and get it working quickly, while also providing enough detail about the board and it's functions so that you can enjoy maximum use of it's features even in the most demanding applications.

When you need help

This manual and all the example programs will provide you with enough information to fully utilize all the features on this board. If you have any problems installing or using this board, contact our Technical support department at <techsupport@rtdfinland.fi>. When sending us an Email request please include the following information: Your company's name and address, your name, your telephone number, and a brief description of the problem.

Chapter 2 - BOARD SETTINGS

The GPS6160HR board has jumper settings, which can be changed to suit your application and host computer configuration. The factory settings are listed and shown in the diagram at the beginning of this chapter. Make sure you completely study and understand this chapter before making changes to these settings.

Factory-Configured Jumper Settings

Table 2-1 below illustrates the factory jumper setting for the GPS6160HR. Figure 2-1 shows the board layout of the GPS6160HR and the locations of the jumpers. The following paragraphs explain how to change the factory jumper settings to suit your specific application.

Table 2-1 Factory configured jumper settings (Please see figure 2-1 below for more detailed locations)

JUMPER NAME	DESCRIPTION	NUMBER OF JUMPERS	FACTORY SETTING
BASE	Base Addresses	6	2E8 / 6E8
IRQ	Host interrupts	11+1	5, G – jumper closed

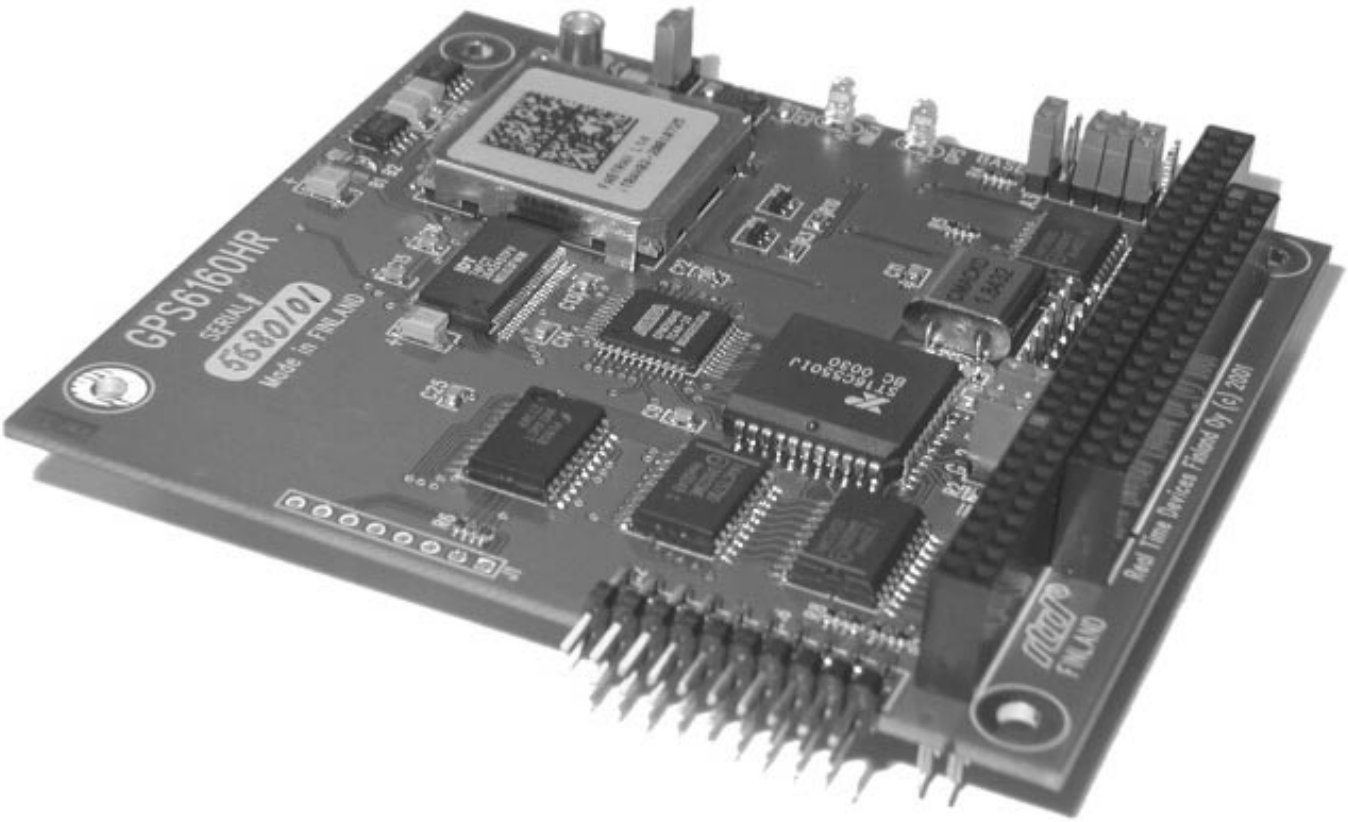

Fig. 2-1 GPS6160HR Board layout showing jumper locations

Base address jumpers (Factory setting: 2E8h / 6E8h)

The GPS6160HR is I/O mapped into the memory space of your host XT/AT. The board occupies a memory window of 8 bytes starting from the base address for UART communication and 4 consecutive bytes starting from BASE+400h for the board control and status registers. As an example if your base address is set to be 2E8h for the serial port, the onboard control registers will start from 6E8h.

The most common cause of failure when you are first setting up your module is address contention: some of your computers I/O space is already occupied by other devices and memory resident programs. When the GPS6160HR attempts to use it's own reserved memory addresses (which are being already used by another peripheral device) erratic performance can occur and the data read from the board may be corrupted.

To avoid this problem make sure you set up the base address by using the six jumpers on the right side of the board, this allows you to choose from a number of different addresses in your host computer's I/O map. Should the factory-installed settings be incompatible to your system configuration, you may change this setting to another using the options illustrated in Table 2-2 (overleaf). The table shows the jumper settings and their corresponding values in hexadecimal form. Ensure that you verify the correct location of the base address jumpers. When the jumper is removed it corresponds to a logical "0", connecting the jumper to a "1". When you set the base address of the module, record the setting inside the back cover of this manual.

GPS6160HR Base address configuration

BASE	A8	A7	A6	A5	A4	A3	BASE	A8	A7	A6	A5	A4	A3
200	0	0	0	0	0	0	300	1	0	0	0	0	0
208	0	0	0	0	0	1	308	1	0	0	0	0	1
210	0	0	0	0	1	0	310	1	0	0	0	1	0
218	0	0	0	0	1	1	318	1	0	0	0	1	1
220	0	0	0	1	0	0	320	1	0	0	1	0	0
228	0	0	0	1	0	1	328	1	0	0	1	0	1
230	0	0	0	1	1	0	330	1	0	0	1	1	0
238	0	0	0	1	1	1	338	1	0	0	1	1	1
240	0	0	1	0	0	0	340	1	0	1	0	0	0
248	0	0	1	0	0	1	348	1	0	1	0	0	1
250	0	0	1	0	1	0	350	1	0	1	0	1	0
258	0	0	1	0	1	1	358	1	0	1	0	1	1
260	0	0	1	1	0	0	360	1	0	1	1	0	0
268	0	0	1	1	0	1	368	1	0	1	1	0	1
270	0	0	1	1	1	0	370	1	0	1	1	1	0
278	0	0	1	1	1	1	378	1	0	1	1	1	1
280	0	1	0	0	0	0	380	1	1	0	0	0	0
288	0	1	0	0	0	1	388	1	1	0	0	0	1
290	0	1	0	0	1	0	390	1	1	0	0	1	0
298	0	1	0	0	1	1	398	1	1	0	0	1	1
2A0	0	1	0	1	0	0	3A0	1	1	0	1	0	0
2A8	0	1	0	1	0	1	3A8	1	1	0	1	0	1
2B0	0	1	0	1	1	0	3B0	1	1	0	1	1	0
2B8	0	1	0	1	1	1	3B8	1	1	0	1	1	1
2C0	0	1	1	0	0	0	3C0	1	1	1	0	0	0
2C8	0	1	1	0	0	1	3C8	1	1	1	0	0	1
2D0	0	1	1	0	1	0	3D0	1	1	1	0	1	0
2D8	0	1	1	0	1	1	3D8	1	1	1	0	1	1
2E0	0	1	1	1	0	0	3E0	1	1	1	1	0	0
2E8	0	1	1	1	0	1	3E8	1	1	1	1	0	1
2F0	0	1	1	1	1	0	3F0	1	1	1	1	1	0
2F8	0	1	1	1	1	1	3F8	1	1	1	1	1	1

0 = JUMPER OFF **1 = JUMPER CLOSED**

Table 2-2 Base address jumper settings for the GPS6160HR, the default jumper settings are highlighted.

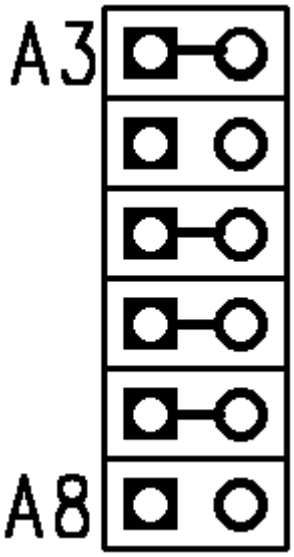

Fig. 2-2 Base address jumpers illustrating address 2E8, A8 is to the bottom, A3 is located to the top of the jumper block

Host interrupts (Factory setting: IRQ5, G closed)

The header connector, shown in Figure 2-3 below, lets you connect the onboard control logic interrupt outputs to one of the interrupt channels available on the host computer XT/AT bus.

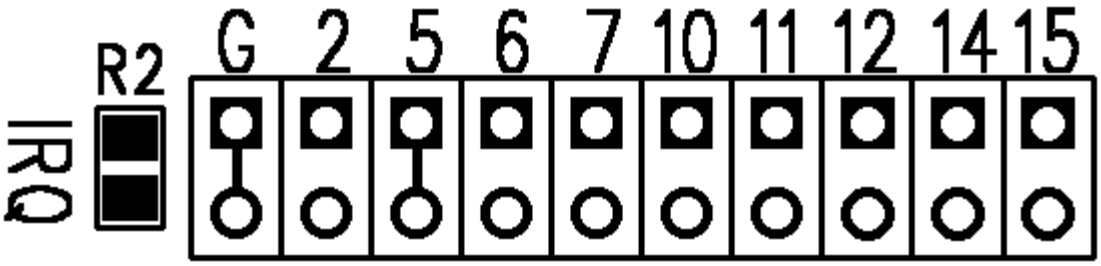

Fig. 2-3 Interrupt jumpers from left to right IRQ2,5,6,7,10,11,12,14,15 and G

Note: The GPS6160HR hardware supports interrupt sharing! Jumper G must be closed on one module per used interrupt. For example if two boards share interrupt number 7 only one board may have the G jumper closed. The G jumper connects a 1KOhm resistor to ground while the shared interrupts are 3-stated pulling the line to an inactive level.

Antenna Bias (Factory setting: +5V)

The three terminal jumper header connector, shown in Figure 2-4 below, lets you connect either +5V or +3,3V to the GPS antenna. This bias voltage is fused with an 80mA quick blow fuse.

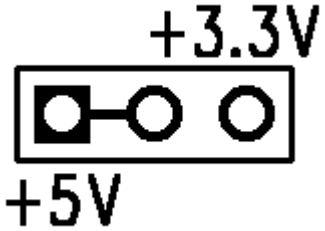

Fig. 2-4 Antenna bias voltage selection jumper

Chapter 3 BOARD INSTALLATION

The GPS6160HR GPS module is designed to directly mount on top or under your RTD PC/104 cpuModule stack. This chapter tells you step-by-step how to install your GPS6160HR into your system.

Board installation

Keep your board in its antistatic bag until you are ready to install it to your system! When removing it from the bag, hold the board at the edges and do not touch the components or connectors. Please handle the board in an antistatic environment and use a **grounded** workbench for testing and handling of your hardware. Before installing the board in your computer, check the power cabling. Failure to do so may cause the power supply unit to malfunction or even cause permanent damage.

General installation guidelines:

- Touch the grounded metal housing of your computer to discharge any antistatic buildup and then remove the board from its antistatic bag.
- Hold the board by the edges and install it in an enclosure or place it on the table on an antistatic surface
- Install your board in your system, and wire the power supply correctly. Failure to do so may cause the power supply unit to malfunction or even cause permanent damage to the device.
- Check all wiring connections once and then once more again
- Check the antenna bias voltage and jumper correctly
- Connect the GPS antenna to the OSX connectors on the GPS6160HR
- Apply power to your system

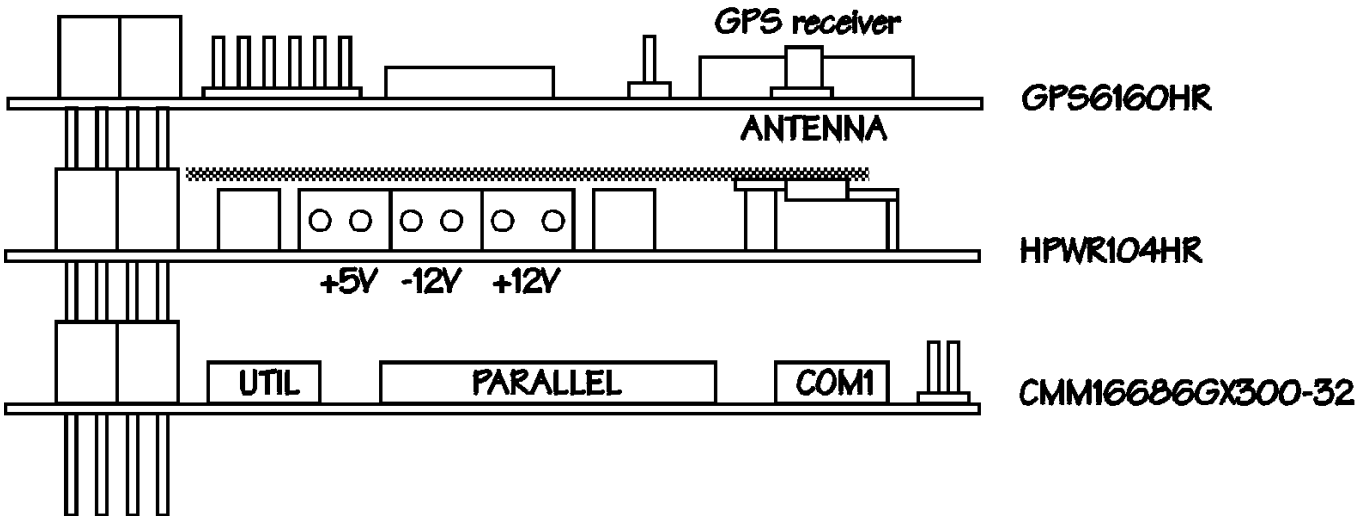

Fig. 3-1 GPS6160HR integrated in a RTD PC/104 cpuModule stack together with a HPWR104HR power supply module and a CMM series cpuModule

General purpose digital I/O connector

The Table 3-1 below shows the pin outs of the GPS6160HR digital I/O interface. The signals in this geader connector can be used as general-purpose TTL level I/O lines to interface to LCD displays, LED's, push buttons or relays. Note that Figure 3-2 shows two connectors together. The connector J16 carries all inputs and J2 carries all the outputs.

PIN J2	**Description**	**PIN J2**	**Description**
1	GND	2	Out0
3	Out1	4	Out2
5	Out3	6	Out4
7	Out5	8	Out6
9	Out7	10	+5V
PIN J16	**Description**	**PIN J16**	**Description**
1	GND	2	In0
3	In1	4	In2
5	In3	6	In4
7	In5	8	In6
9	In7	10	+5V

Table 3-1 Pin outs of the GPS6160HR digital I/O interface connector

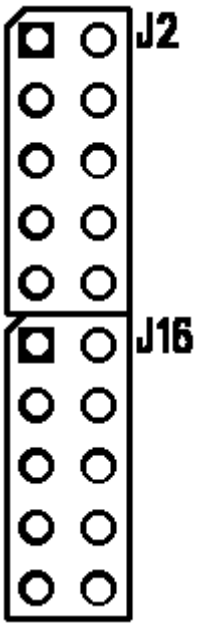

Fig 3-2 Digital I/O connector layout of the GPS6160HR

Chapter 4 - HARDWARE DESCRIPTION

This chapter describes the major hardware building blocks of the GPS6160HR:

- GPS receiver module
- GPS antenna considerations
- UART serial port circuitry
- Digital I/O
- Status LED's

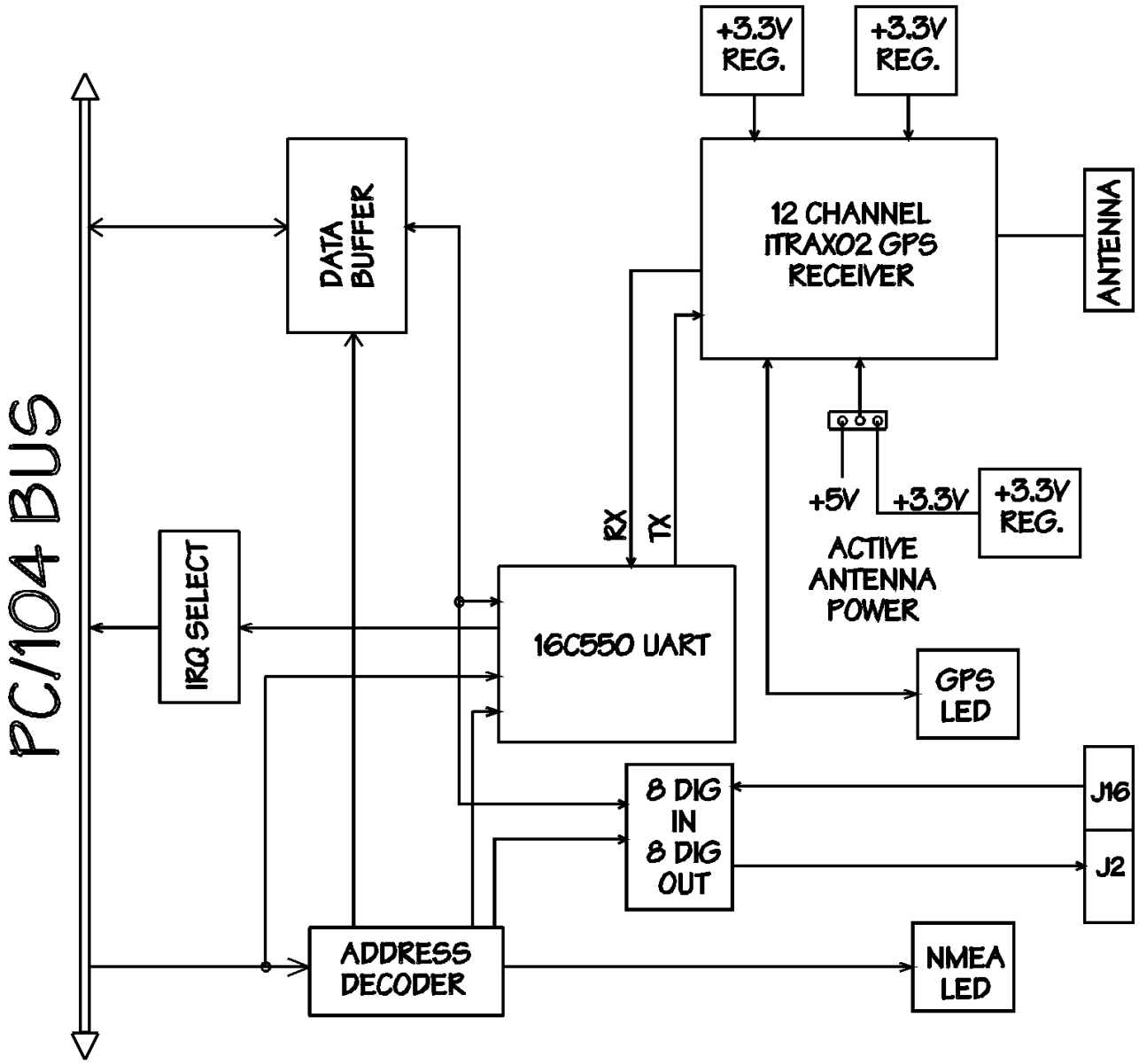

Fig. 4-1 Block diagram of the GPS6160HR

GPS receiver

Intergarated on the GPS6160HR is an iTrax02 low power fast-fix 12-channel GPS receiver from Fastrax. This GPS receiver is especially designed for portable and mobile applications. This version of the GPS does not support differential operation. RTD Finland can also provide solutions for indoor navigation using pseudolites (Pseudo Satellite) instead of satellites in the sky for positioning. In this case the standard GPS receiver can be subsitituted by a pseudolite receiver. Application areas include warehouse navigation.

The iTrax02 sensitivity provides continuous tracking and navigation down to a signal level of –145 dBm and a cold start TTFF of 50 seconds (no initialisation), 30 seconds for warm start (almanac) and one second for quick start. Even with this performance the power consumption is approximately 100mW with a 1s update-rate. This figure does not include the active antenna power consumption. A complete GPS configuration program for the iTrax02 GPS Workbench is available from the manufacturer's website at http://www.fastrax.fi/. This program allows you to completely reconfigure the operation of the GPS receive. To use this program you must configure the GPS to operate in iTalk protocol using the RTD GPS diagnostics program.

GPS data is output only when the receiver has a fix. The GPS6160HR is configured to output NMEA-0183 Ver 3.0 data after reset and can be changed to binary protocol through a bit in the control register.

GPS Antenna considerations

GPS active antennas are mostly active today. The GPS6160HR accepts either +5V or +3,3V active GPS antennas. A three-terminal header is used to select the oprating voltage of the antenna. The internal gain of the GPS receiver can be programmably adjusted to low-output signals or even to interface to passive antennas. This operation is normally not needed, but it can be done using the Fastrax GPS Workbench program.

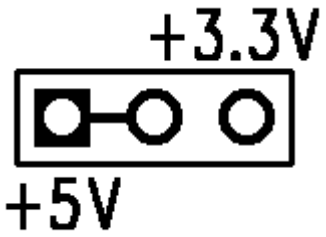

Fig. 4-2 GPS antenna bias voltage

A 90 degree 50 Ohm OSX connector should be selected to directly plug into the antenna connector on the board. High quality low loss antenna cable should be used. Try to reduce the number of connectors on the cable to minimise signal reflections. Signal reflections on the antenna line may cause incorrect readings for altitude information.

UART serial port circuitry

GPS data is sent and received through a standard 16C550 compatible UART. All today's operating systems will recognize and support this serial communication device. The GPS6160HR uses its own onboard serial port and will not reserve serial port resources from the system. The I/O base address and interrupts for the serial port can be flexibly set as has been described in previous chapters of this manual. This user's manual will not wade into details of serial port programming. This information is commonly available today. You can use any communication software package or terminal program to connect to your GPS6160HR UART. Just make sure you set up the I/O and IRQ right. The UART on the board is specified for full operation from –40 to +85C. The oscillator frequency is set to be 1.8432MHz. Note that the UART interrupt can be disabled or enabled from software by writing to bit 01 in address BASE+0x402.

The GPS receiver has two available protocols. You may select to use either the NMEA protocol or alternatively the iTalk binary protocol. The GPS receiver has two internal serial ports that operate in parallel. These outputs are multiplexed into the 16C550 UART channel on the GPS6160HR board. You may change between protocols by writing to a control bit in the internal registers of the board. This will be described in the later chapters of this manual.

Digital I/O

For general-purpose digital I/O interfacing a 16-bit digital I/O port is provided. This port includes 8 TTL-level digital outputs that are cleared (to 0) after system reset. Also are included 8 digital inputs with 10K Ohm pull-down resistors. These I/O's are located on the left side of the board. These I/O's are ideal to be used to interface to LCD displays, LED's push buttons or other low power controls.

Status-LEDs

Two status-LEDs are provided for easy system status detection. One LED shows the selected protocol. The other LED indicates the GPS tracking status. Figure 4-3 below shows the location of the two LEDs.

NMEA	On	-> NMEA protocol currently selected
	Off	-> iTalk protocol currently selected
GPS	Blinking	-> GPS receives signal and is tracking satellites
	Off	-> GPS fix, tacking and all coordinates are valid.

Chapter 5 BOARD OPERATION AND PROGRAMMING

This chapter shows you how to program and use your GPS6160HR. It provides a general description of the I/O map. Detailed serial port programming tips are not within the scope of this manual.

Defining the Memory Map

The memory map of the GPS6160HR occupies a group of eight bytes of host PC I/O space. This window is freely selectable by the user as described in *Chapter 2, Table 2-2.* After setting the base address you have access to the internal resources of the GPS6160HR control logic. These resources are not described in detail, since they are mapped as a standard PC serial port. For more details on the EXAR ST16C550IJ44 UART chip programming please download the component specific data from the website: http://www.exar.com/products/st16c550.html

ADDR (hex)	REGISTER	DIR	COMMENTS
BASE	TXD	O	Only if control reg. Bit 7=0
	RXD	I	Only if control reg. Bit 7=0
	BAUD div. Low		Only if control reg. Bit 7=1
BASE+1	BAUD div. High		Only if control reg. Bit 7=1
	IRQ enable		Only if control reg. Bit 7=0
BASE+2	IRQ ID		
BASE+3	Line control		
BASE+4	Modem control		
BASE+5	Line status		
BASE+6	Modem status		
BASE+400	Digital I/O	I/O	Digital I/O port
BASE+401	GPS status	I/O	Configuration registers
RESERVED			

Table 5-1 General I/O map of the GPS6160HR GPS UART

BASE+400 Digital I/O (R/W)

This address is used to interface to the digital I/O port of the GPS6160HR, writing to this address will transfer the data out of the output port, while reading from this address will return the data from the digital inputs.

BASE+401 GPS Status (R/W, 0x00 after reset)

Write

Bit 0	CH_SEL	0 – NMEA mode; 1 – iTalk protocol
Bit 1	GPS_RESET	1 – Hard reset of GPS receiver, 0 – active
Bit 2	RESERVED	
Bit 3	/EN_INT	0 – GPS interrupt enabled; 1 – disabled

Read

Bit 0	CH_SEL	state	
Bit 1	GPS_RESET	state	
Bit 2	GPIO8 of GPS	state	(Reserved for future use and testing)
Bit 3	/EN_INT	state	

INTERRUPTS

What is an interrupt?

An interrupt is an event that causes the processor in your computer to temporarily halt its current process and execute another routine. Upon completion of the new routine, control is returned to the original routine at the point where its execution was interrupted.

Interrupts are a very flexible way of dealing with asynchronous events. Keyboard activity is a good example; your computer cannot predict when you might press a key and it would be a waste of processor time to do nothing whilst waiting for a keystroke to occur. Thus the interrupt scheme is used and the processor proceeds with other tasks. When a keystroke finally occurs, the keyboard then 'interrupts' the processor so that it can get the keyboard data. It then places it into the memory, and then returns to what it was doing before the interrupt occurred. Other common devices that use interrupts are A/D boards, network boards, other used serial ports etc.

Interrupt request lines

To allow different peripheral devices to generate interrupts on the same computer, the PC AT bus has interrupt request channels (IRQ's). A rising edge transition on one of these lines will be latched into the interrupt controller. The interrupt controller checks to see if the interrupts are to be acknowledged from that IRQ and, if another interrupt is being processed, it decides if the new request should supercede the one in progress or if it has to wait until the one in progress has been completed. The priority level of the interrupt is determined by the number of the IRQ as follows; IRQ0 has the highest priority whilst IRQ15 has the lowest. Many of the IRQ's are already used by the standard system resources, IRQ0 is dedicated to the internal timer, IRQ1 is dedicated to the keyboard input, IRQ3 for the serial port COM2, and IRQ4 for the serial port COM1. Often interrupts 2,5,7,10,11 and 15 are free for the user.

8259 Programmable Interrupt Controller

The chip responsible for handling interrupt requests in a PC is the 8259 Interrupt Controller. To use interrupts you will need to know how to read and set the 8259's internal interrupt mask register (IMR) and how to send the end-of-interrupt (EOI) command to acknowledge the 8259 interrupt controller.

Interrupt Mask Register (IMR)

Each bit in the interrupt mask register (IMR) contains the mask status of the interrupt line. If a bit is set (equal to 1), then the corresponding IRQ is masked, and it will not generate an interrupt. If a bit is cleared (equal to 0), then the corresponding IRQ is not masked, and it can then generate an interrupt. The interrupt mask register is programmed through **port 21h**.

End-of-Interrupt (EOI) Command

After an interrupt service routine is complete, the 8259 Interrupt Controller must be acknowledged by writing the value 20h to port 20h.

What exactly happens when an interrupt occurs?

Understanding the sequence of events when an interrupt is triggered is necessary to correctly write interrupt handlers. When an interrupt request line is driven high by a peripheral device (such as the GPS6160HR), the interrupt controller checks to see if interrupts are enabled for that IRQ. It then checks to see if other interrupts are active or requested and determines which interrupt has priority. The interrupt controller then

interrupts the processor. The current code segment (CS), instruction pointer (IP), and flags are pushed onto the system stack, and a new set if CS and IP are loaded from the lowest 1024 bytes of memory.

This table is referred to as the interrupt vector table and each entry to this table is called an interrupt vector. Once the new CS and IP are loaded from the interrupt vector table, the processor starts to execute code from the new Code Segment (CS) and from the new Instruction Pointer (IP). When the interrupt routine is completed, the old CS and IP are popped from the system stack and the program execution continues from the point where interruption occurred.

Using Interrupts in your Program

Adding interrupt support to your program is not as difficult as it may seem especially when programming under DOS. The following discussion will cover programming under DOS. Note that even the smallest mistake in your interrupt program may cause the computer to hang up and will only restart after a reboot. This can be frustrating and time-consuming.

Writing an Interrupt Service Routine (ISR)

The first step in adding interrupts to your software is to write an interrupt service routine (ISR). This is the routine that will be executed automatically each time an interrupt request occurs for the specified IRQ. An ISR is different from other sub-routines or procedures. First on entrance the processor registers must be pushed onto the stack before anything else! Second, just before exiting the routine, you must clear the interrupt on the GPS6160HR by writing to the Status register, and write the EOI command to the interrupt controller. Finally, when exiting the interrupt routine the processor registers must be popped from the system stack and you must execute the IRET assembly instruction. This instruction pops the CS, IP and processor flags from the system stack. These were pushed onto the stack when entering the ISR.

Most compilers allow you to identify a function as an interrupt type and will automatically add these instructions to your ISR with one exception: most compilers do not automatically add the EOI command to the function, you must do it yourself. Other than this and a few exceptions discussed below, you can write your ISR as any code routine. It can call other functions and procedures in your program and it can access global data. If you are writing your first ISR, we recommend you stick to the basics; just something that enables you to verify you have entered the ISR and executed it successfully. For example: set a flag in your ISR and in your main program check for the flag.

Note: If you choose to write your ISR in in-line Assembly, you must push and pop registers correctly and exit the routine with the IRET instruction instead of the RET instruction.

There are a few precautions you must consider when writing ISR's. The most important is, **do not use any DOS functions or functions that call DOS functions from an interrupt routine.** DOS is not re-entrant; that is, a DOS function cannot call itself. In typical programming, this will not happen because of the way DOS is written. But what about using interrupts? Consider then the following situation in your program: If DOS function X is being executed when an interrupt occurs and the interrupt routine makes a call to the same DOS function X, then function X is essentially being called while active. Such cases will cause the computer to crash. DOS does not support such operations. The general rule is that do not call any functions that use the screen, read keyboard input or any file I/O routines, these should not be used in ISR's.

The same problem of re-entrancy also exists for many floating-point emulators. This effectively means that you should also avoid floating point mathematical operations in your ISR.

Note that the problem of reentrancy exists, no matter what programming language you use. Even, if you are writing your ISR in Assembly language, DOS and many floating point emulators are not re-entrant. Of course there are ways to avoid this problem, such as those which activate when your ISR is called. Such solutions are, however, beyond the scope of this manual.

The second major concern when writing ISR's is to make them as short as possible in term of execution time. Spending long times in interrupt service routines may mean that other important interrupts are not serviced. Also, if you spend too long in your ISR, it may be called again before you have exited. This will lead to your computer hanging up and will require a reboot.

Your ISR should have the following structure:

- Push any processor registers used in your ISR.
- Put the body of your routine here
- Clear the interrupt bit by reading GPS6160HR RXD register
- Issue the EOI command to the 8259 by writing 20h to 20h
- Pop all registers. Most C compilers do this automatically

The following C example shows what the shell of your ISR should be like:

```
/*---------------------------------------------------------------------------
| Function:    new_IRQ_handler
| Inputs:      Nothing
| Returns:     Nothing
|---------------------------------------------------------------------------*/
void interrupt far new_IRQ_handler(void)
{
        IRQ_flag = 1;          // Indicate to process interrupt has occurred

        {
                               // Your program code to read UART
                               // read to a data buffer for example:
        Guc_buffer[Gi_bufpos++] = inp(gi_SERIAL_DATA);
        }
        outp(0x20, 0x20);      // Acknowledge the interrupt controller
}
```

Saving the Startup Interrupt Mask Register (IMR) and interrupt vector

The next step after writing the ISR is to save the startup-state of the interrupt mask register, (IMR) and the original interrupt vector you are using. The IMR is located in address 21h. The interrupt vector you will be using is located in the interrupt vector table which is an array of pointers (addresses) and it is locate din the first 1024 bytes of the memory (Segment 0 offset 0). You can read this value directly, but it is better practice to use DOS function 35h (get interrupt vector) to do this. Most C compilers have a special function available for doing this. The vectors for the hardware interrupts on the XT - bus are vectors 8-15, where IRQ0 uses vector 8 and IRQ7 uses vector 15. Thus if your GPS6160HR is using IRQ5 it corresponds to vector number 13.

Before you install your ISR, temporarily mask out the IRQ you will be using. This prevents the IRQ from requesting an interrupt while you are installing and initializing your ISR. To mask the IRQ, read the current IMR at I/O port 21h, and set the bit that corresponds to the IRQ. The IMR is arranged so that bit 0 is for IRQ0 and bit 7 is for IRQ7. See the paragraph entitled *Interrupt Mask Register (IMR*) earlier in this discussion for help in determining your IRQ's bit. After setting the bit, write the new value to I/O port 21h.

With the startup IMR saved and the interrupts temporarily disabled, you can assign the interrupt vector to point to your ISR. Again you can overwrite the appropriate entry in the vector table with a direct memory write, but this is not recommended. Instead use the DOS function 25h (Set Interrupt Vector) or, if your compiler provides it, the library routine for setting up interrupt vectors. Remember that interrupt vector 8 corresponds to IRQ0, vector 9 for IRQ1 etc.

If you need to program the source of your interrupts, do that next. For example, if you are using transmitted or received messages as an interrupt source program it to do that. Finally, clear the mask bit for your IRQ in the IMR. This will enable your IRQ.

Common Interrupt mistakes

Remember hardware interrupts are from 8-15, XT IRQ's are numbered 0-7. Do not forget to clear the IRQ mask bit in the IMR Forgetting to send the EOI command after ISR code. Disables further interrupts.

Example on Interrupt vector table setup in C-code:

```
void far _interrupt new_IRQ1_handler(void );            /* ISR function */
#define IRQ1_VECTOR     3                               /* Name for IRQ */
void (interrupt far *old_IRQ1_dispatcher)
        (es,ds,di,si,bp,sp,bx,dx,cx,ax,ip,cs,flags);    /* Variable to store
old IRQ_Vector */
void far _interrupt new_IRQ1_handler(void );

/*---------------------------------------------------------------------
| Function:    init_irq_handlers
| Inputs:      Nothing
| Returns:     Nothing
| Purpose:     Set the pointers in the interrupt table to point to
|              our funtions ie. setup for ISR's.
|---------------------------------------------------------------------*/
void init_irq_handlers(void)
{
        _disable();
                old_IRQ1_handler = _dos_getvect(IRQ1_VECTOR + 8);
                _dos_setvect(IRQ1_VECTOR + 8, new_IRQ1_handler);
                Gi_old_mask = inp(0x21);
                outp(0x21,Gi_old_mask & ~(1 << IRQ1_VECTOR));
        _enable();
}
```

```
|/*---------------------------------------------------------------------
| Function:    restore, do this before exiting program
| Inputs:      Nothing
| Returns:     Nothing
| Purpose:     Restore the interrupt vector table.
|---------------------------------------------------------------------*/
void restore(void)
{
        /* Restore the old vectors */
        _disable();

                _dos_setvect(IRQ1_VECTOR + 8, old_IRQ1_handler);
                outp(0x21,Gi_old_mask);

        _enable();
}
```

Chapter 6 - GPS6160HR SPECIFICATIONS

Host interface

16-bit PC/104 bus, XT-bus used for data

GPS specifications

General

L1 frequency, C/A code (SPS)
12 independent tracking channels
Separate search and acquisition engines

Update rate	1fix/s or configurable
Accuracy	Position 10m CEP (50%) 0.2 m/s (50%)
Sensitivity	-145dBm
Status indicator	1 LED

Antenna Interface

External	Passive or active +3,3V or +5,0V BIAS
Connector	OSX, PCB mount

UART and I/O

UART compatibility	16C550
Oscillator frequency	1.8432MHz
Connection	TX and RX only
Base addresses	32
Interrupts	2,5,7,10,11,12,14 and 15
Digital I/O	8 TTL outputs, 8 TTL inputs w. 10K pull-down

GPS6160HR Electromechanical

Operating temperature range	-40 to +85C
Humidity	RH up to 95% non condensing
Altitude	-1000 to 60.000 ft
Vibration	Survival 10G peak
Power consumption	1,3W min

Chapter 7 - RETURN POLICY AND WARRANTY

Return Policy

If the module requires repair, you may return it to us by following the procedure listed below:

Caution:	Failure to follow this return procedure will *almost always* delay repair! Please help us expedite your repair by following this procedure.

1) Read the limited warranty, which follows.

2) Contact the factory and request a Returned Merchandise Authorization (RMA) number.

3) On a sheet of paper, write the name, phone number, and fax number of a technically competent person who can answer questions about the problem.

4) On the paper, write a detailed description of the problem with the product. Answer the following questions:

- Did the product ever work in your application?
- What other devices were connected to the product?
- How was power supplied to the product?
- What features did and did not work?
- What was being done when the product failed?
- What were environmental conditions when the product failed?

5) Indicate the method we should use to ship the product back to you.

- We will return warranty repairs by UPS Ground at our expense.
- Warranty repairs may be returned by a faster service at your expense.
- Non-warranty repairs will be returned by UPS Ground or the method you select, and will be billed to you.

6) Clearly specify the address to which we should return the product when repaired.

7) Enclose the paper with the product being returned.

8) Carefully package the product to be returned *using anti-static packaging!* We will not be responsible for products damaged in transit for repair.

7) Write the RMA number on the outside of the package.

8) Ship the package to:

Real Time Devices Finland Oy

Lepolantie 14

FIN-00660 Helsinki

FINLAND

Limited Warranty

Real Time Devices, Inc. warrants the hardware and software products it manufactures and produces to be free from defects in materials and workmanship for one year following the date of shipment from REAL TIME DEVICES. This warranty is limited to the original purchaser of product and is not transferable.

During the one year warranty period, REAL TIME DEVICES will repair or replace, at its option, any defective products or parts at no additional charge, provided that the product is returned, shipping prepaid, to REAL TIME DEVICES. All replaced parts and products become the property of REAL TIME DEVICES. Before returning any product for repair, customers are required to contact the factory for an RMA number.

THIS LIMITED WARRANTY DOES NOT EXTEND TO ANY PRODUCTS WHICH HAVE BEEN DAMAGED AS A RESULT OF ACCIDENT, MISUSE, ABUSE (such as: use of incorrect input voltages, improper or insufficient ventilation, failure to follow the operating instructions that are provided by REAL TIME DEVICES, "acts of God" or other contingencies beyond the control of REAL TIME DEVICES), OR AS A RESULT OF SERVICE OR MODIFICATION BY ANYONE OTHER THAN REAL TIME DEVICES. EXCEPT AS EXPRESSLY SET FORTH ABOVE, NO OTHER WARRANTIES ARE EXPRESSED OR IMPLIED, INCLUDING, BUT NOT LIMITED TO, ANY IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE, AND REAL TIME DEVICES EXPRESSLY DISCLAIMS ALL WARRANTIES NOT STATED HEREIN. ALL IMPLIED WARRANTIES, INCLUDING IMPLIED WARRANTIES FOR MECHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE, ARE LIMITED TO THE DURATION OF THIS WARRANTY. IN THE EVENT THE PRODUCT IS NOT FREE FROM DEFECTS AS WARRANTED ABOVE, THE PURCHASER'S SOLE REMEDY SHALL BE REPAIR OR REPLACEMENT AS PROVIDED ABOVE. UNDER NO CIRCUMSTANCES WILL REAL TIME DEVICES BE LIABLE TO THE PURCHASER OR ANY USER FOR ANY DAMAGES, INCLUDING ANY INCIDENTAL OR CONSEQUENTIAL DAMAGES, EXPENSES, LOST PROFITS, LOST SAVINGS, OR OTHER DAMAGES ARISING OUT OF THE USE OR INABILITY TO USE THE PRODUCT.

SOME STATES DO NOT ALLOW THE EXCLUSION OR LIMITATION OF INCIDENTAL OR CONSEQUENTIAL DAMAGES FOR CONSUMER PRODUCTS, AND SOME STATES DO NOT ALLOW LIMITATIONS ON HOW LONG AN IMPLIED WARRANTY LASTS, SO THE ABOVE LIMITATIONS OR EXCLUSIONS MAY NOT APPLY TO YOU.

THIS WARRANTY GIVES YOU SPECIFIC LEGAL RIGHTS, AND YOU MAY ALSO HAVE OTHER RIGHTS, WHICH VARY FROM STATE TO STATE.